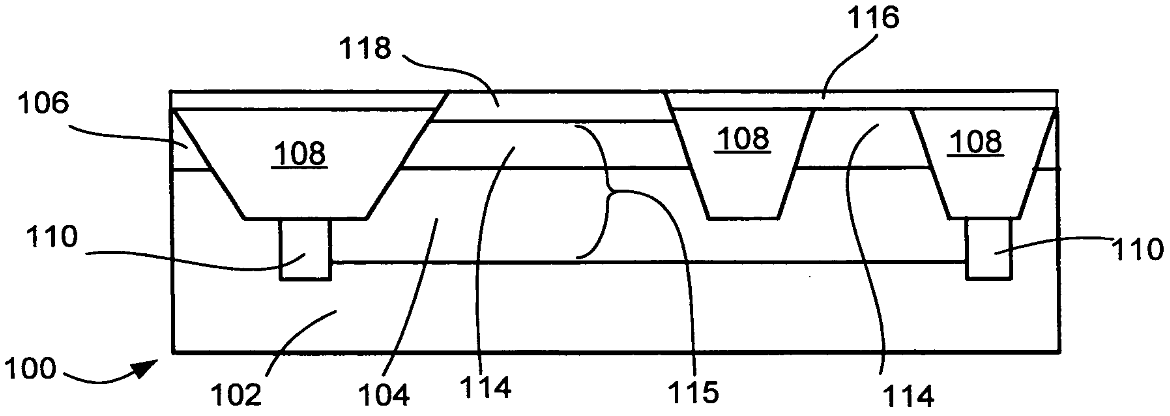

FIG. 1

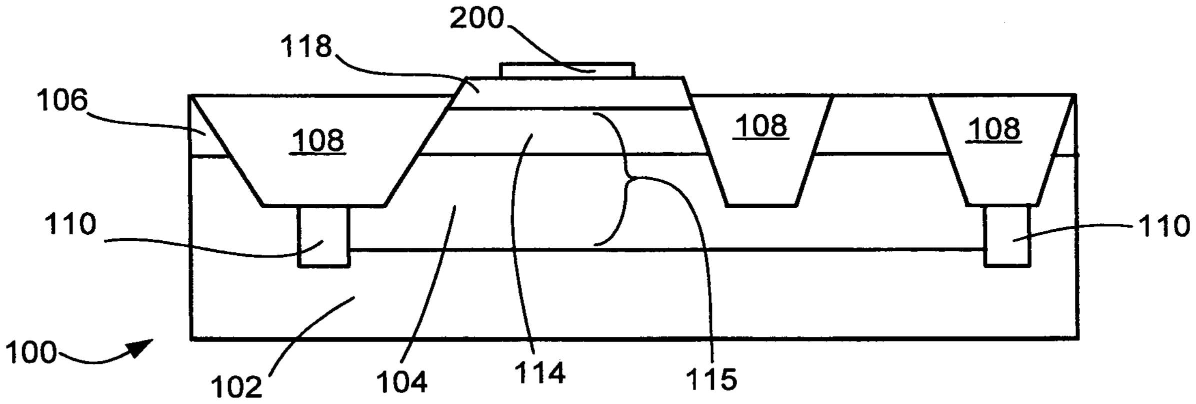

FIG. 2

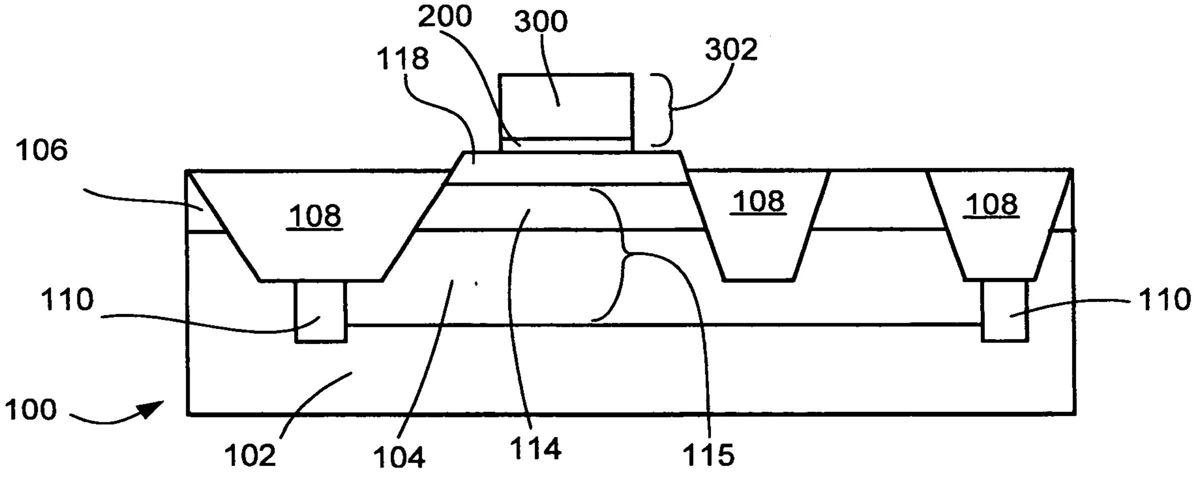

FIG. 3

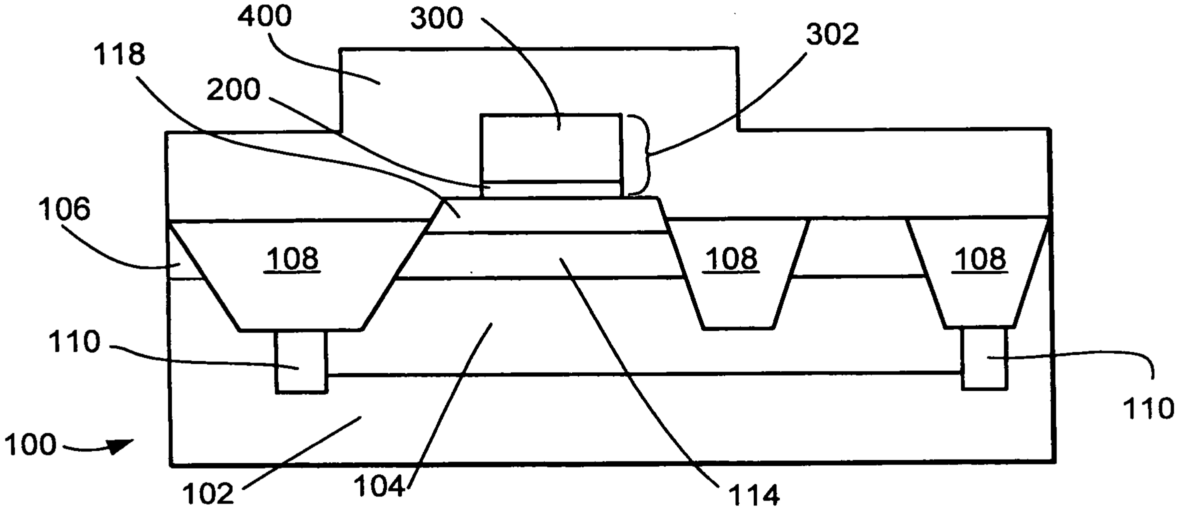

FIG. 4

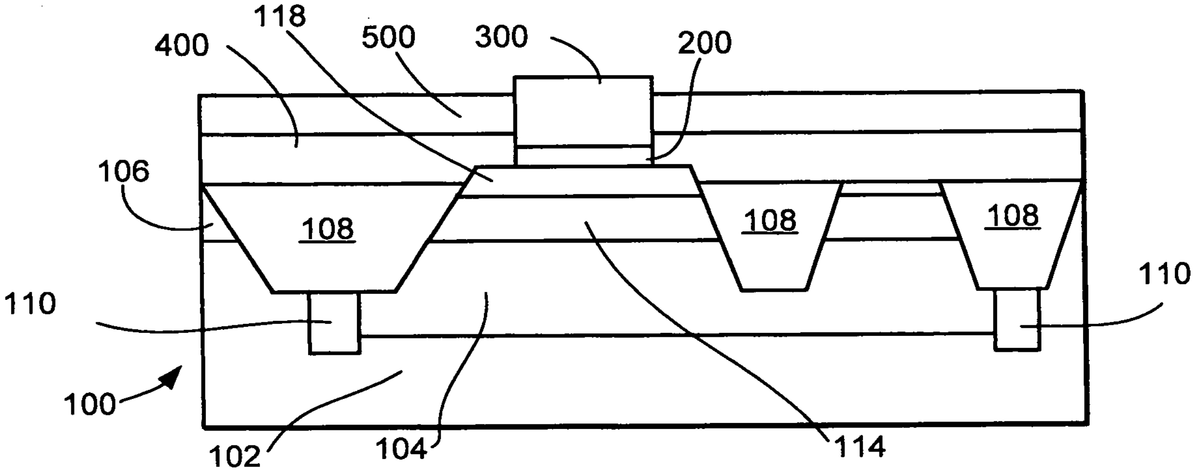

FIG. 5

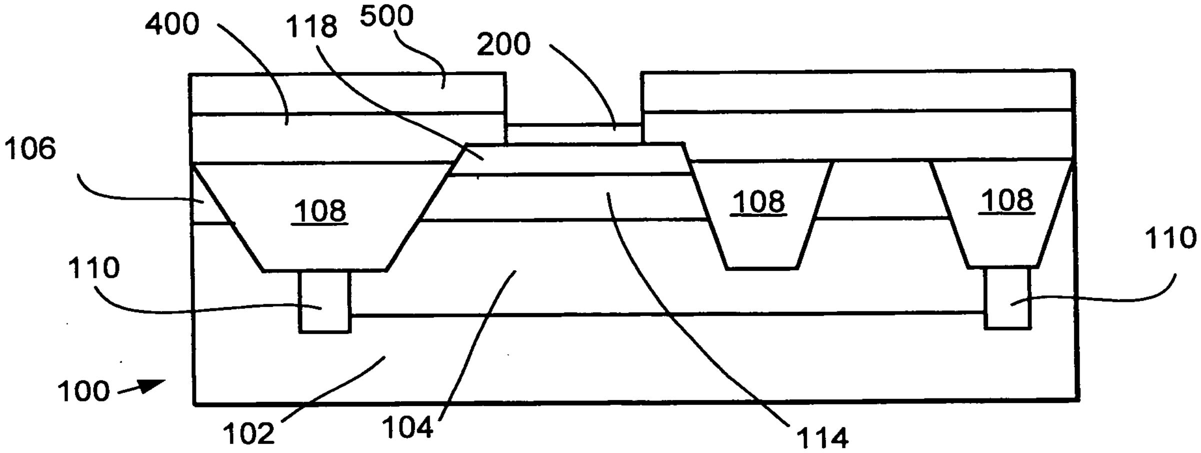

FIG. 6

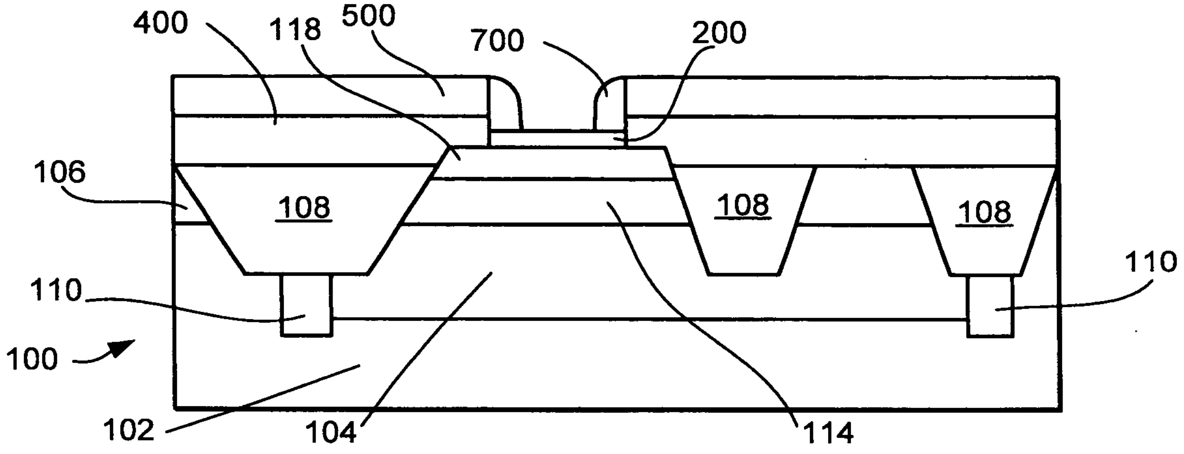

FIG. 7

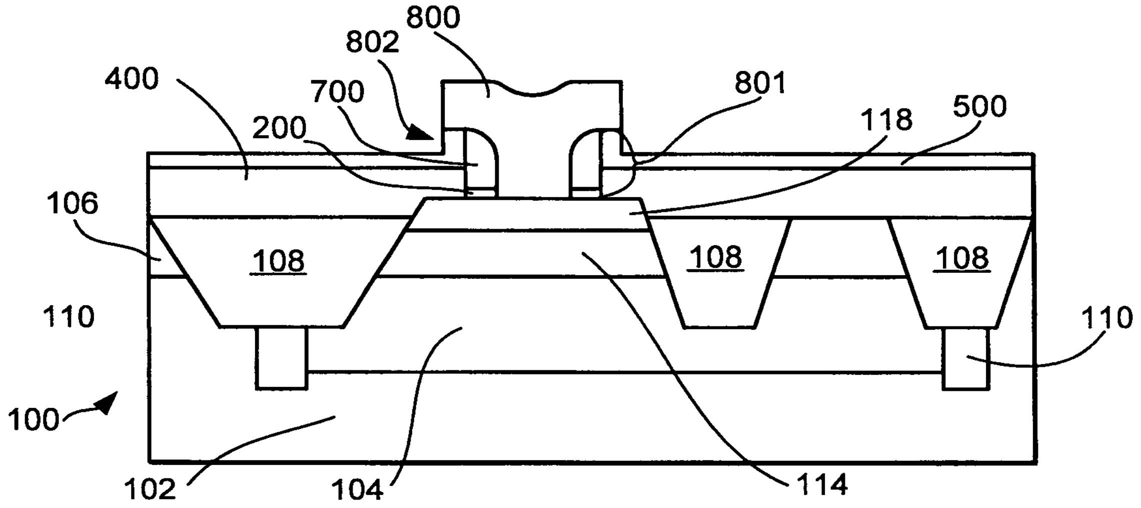

FIG. 8

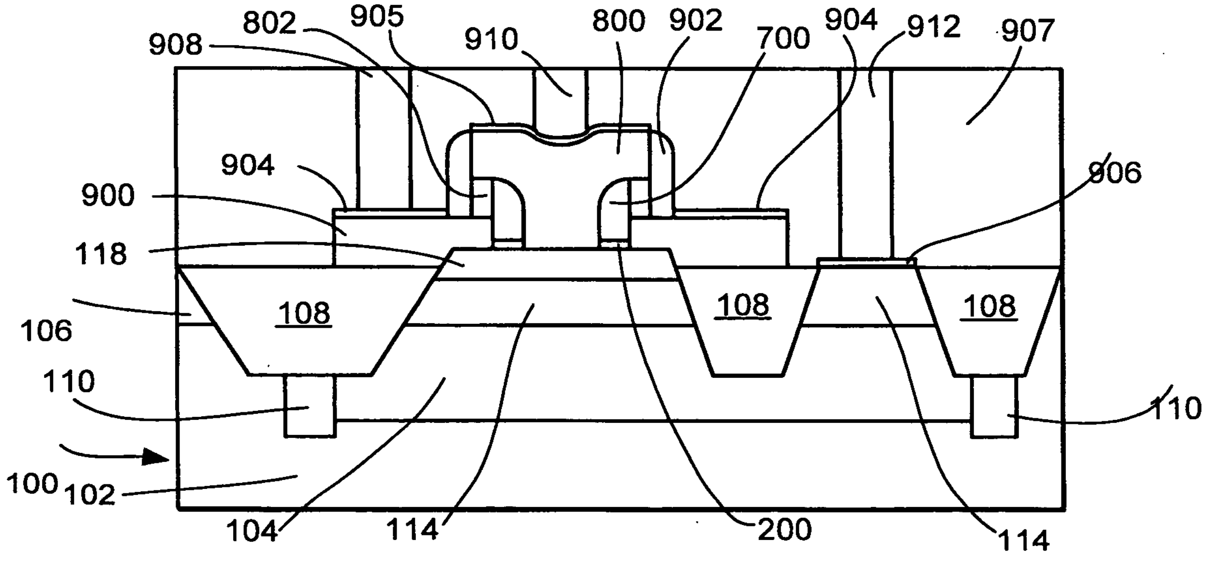

FIG. 9

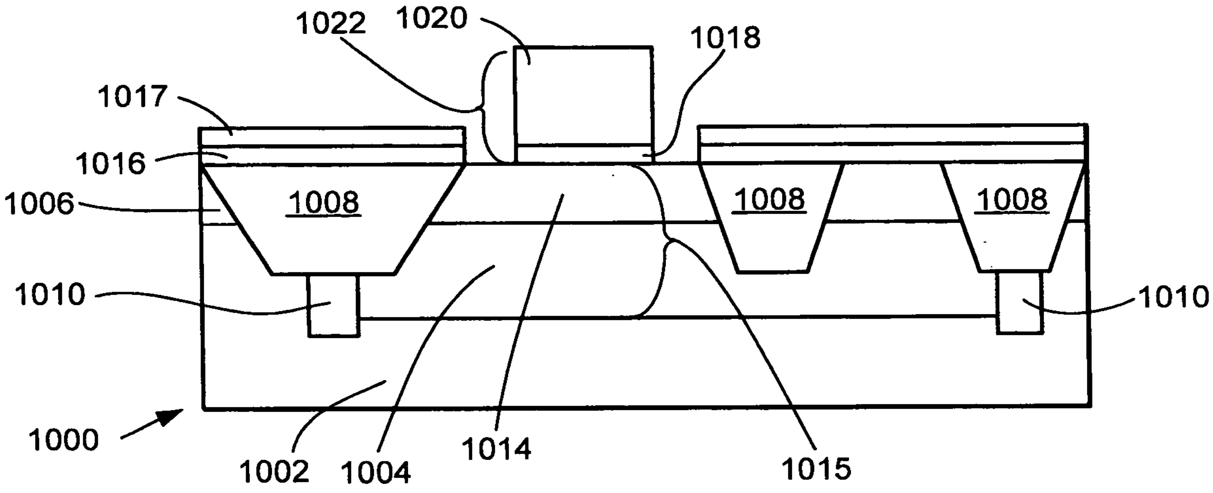

FIG. 10

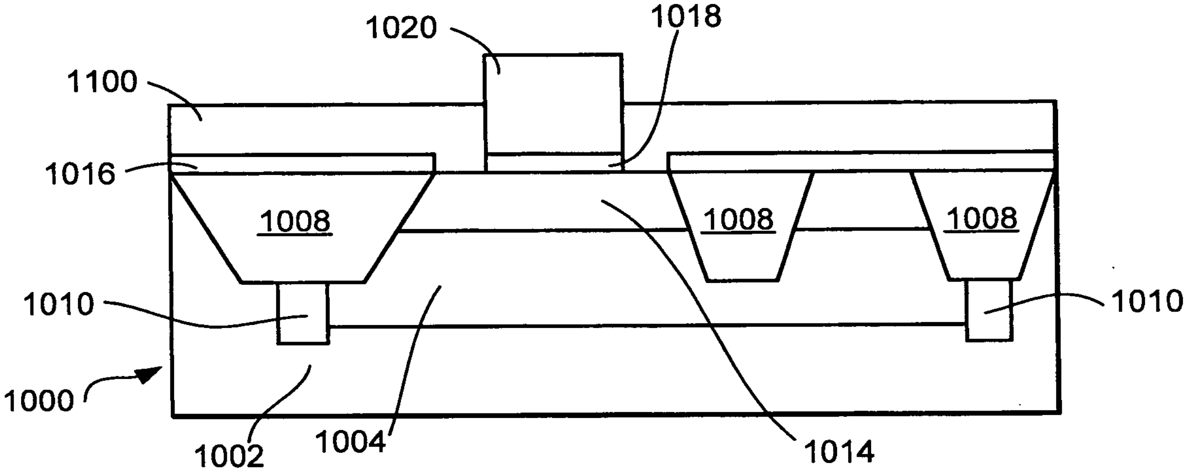

FIG. 11

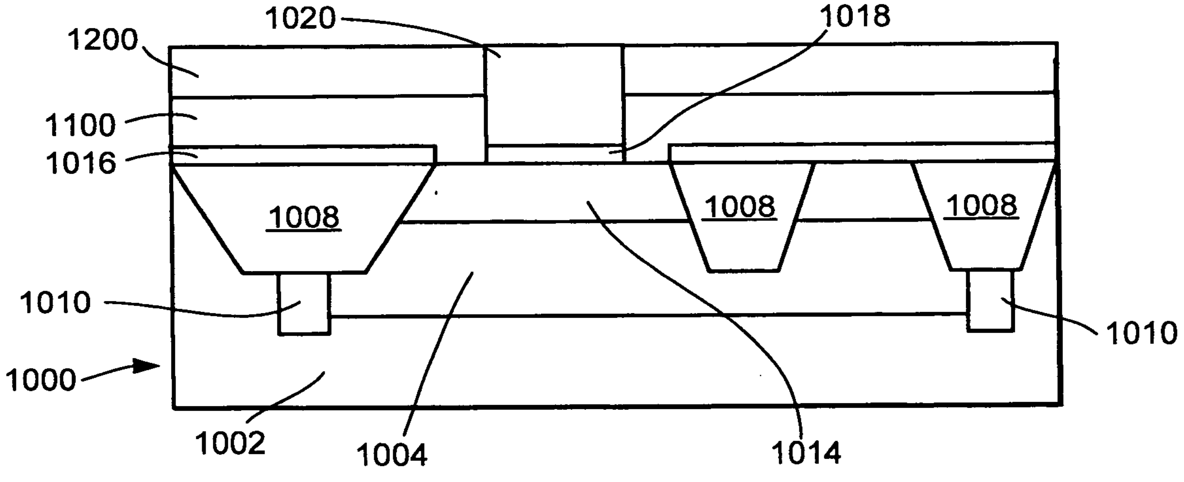

FIG. 12

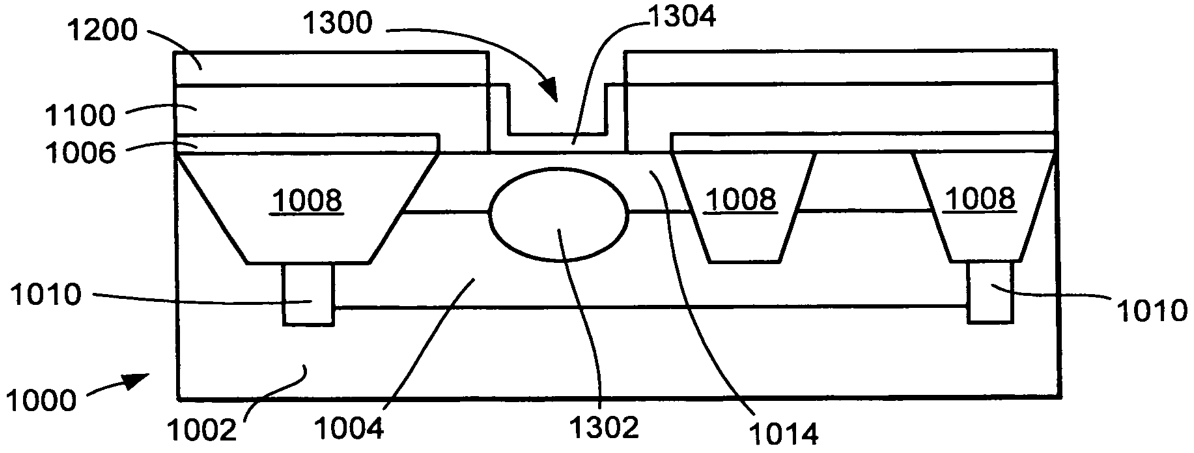

FIG. 13

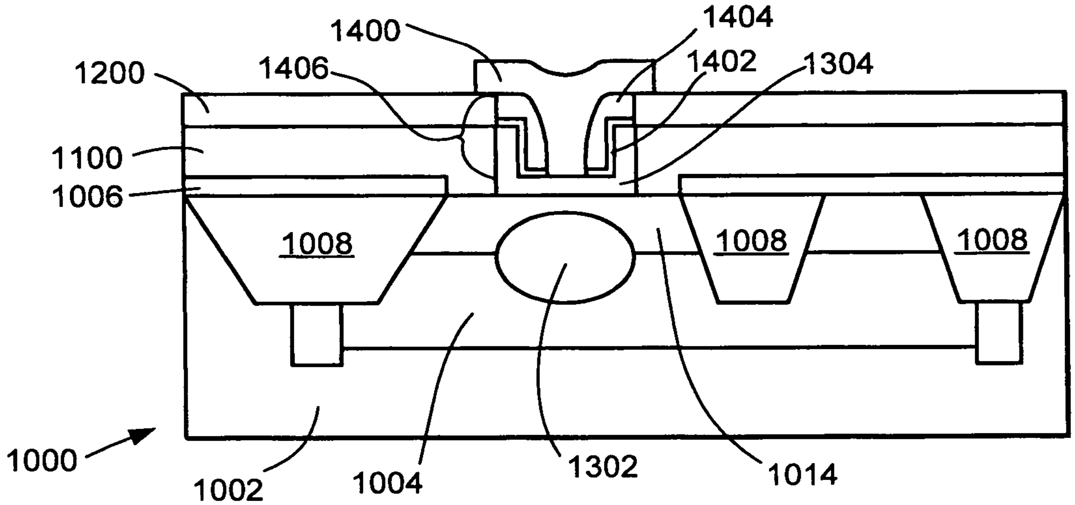

FIG. 14

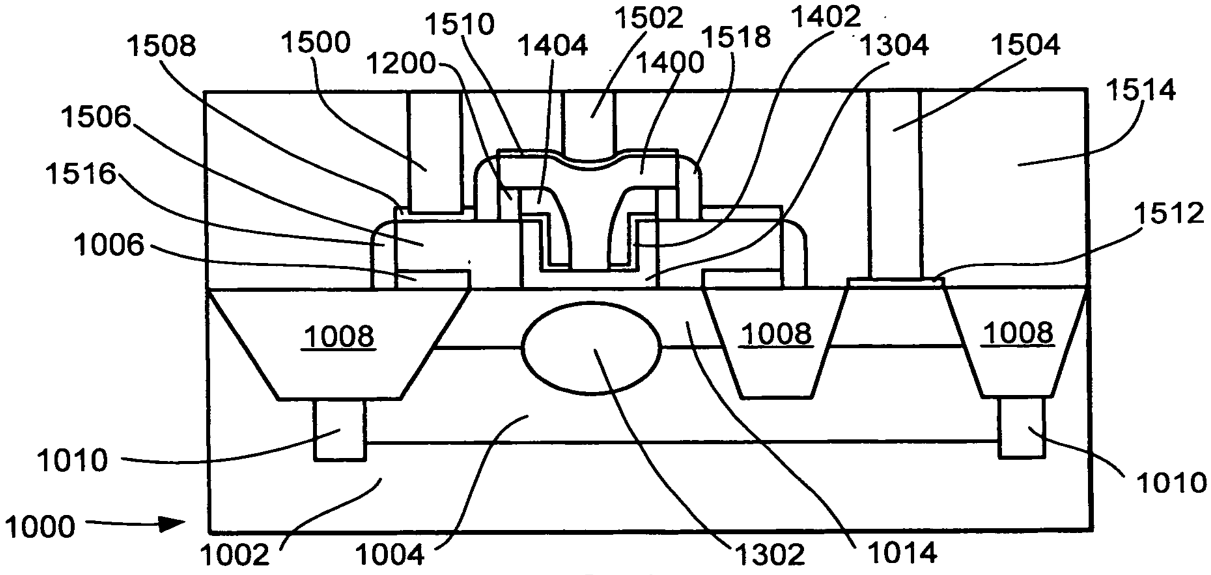

FIG. 15

Page 6of 10
Title: HETEROJUNCTION BIPOLAR TRANSISTOR
USING REVERSE EMITTER WINDOW
Inventors: Purakh Raj Verma, et al.
Docket No.: 1016-031
Contact: Mikio Ishimaru (408) 738-0592

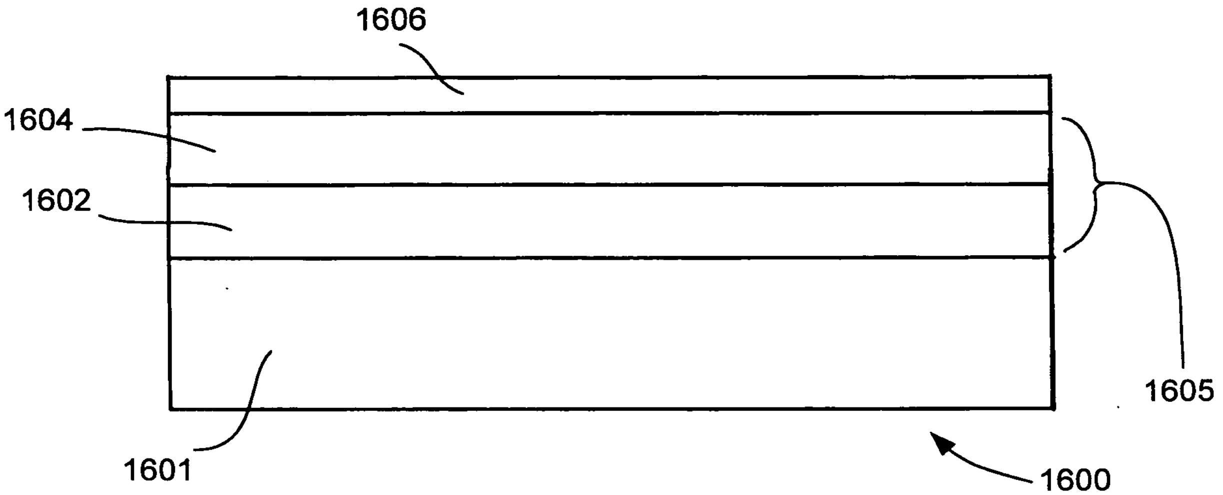

FIG. 16

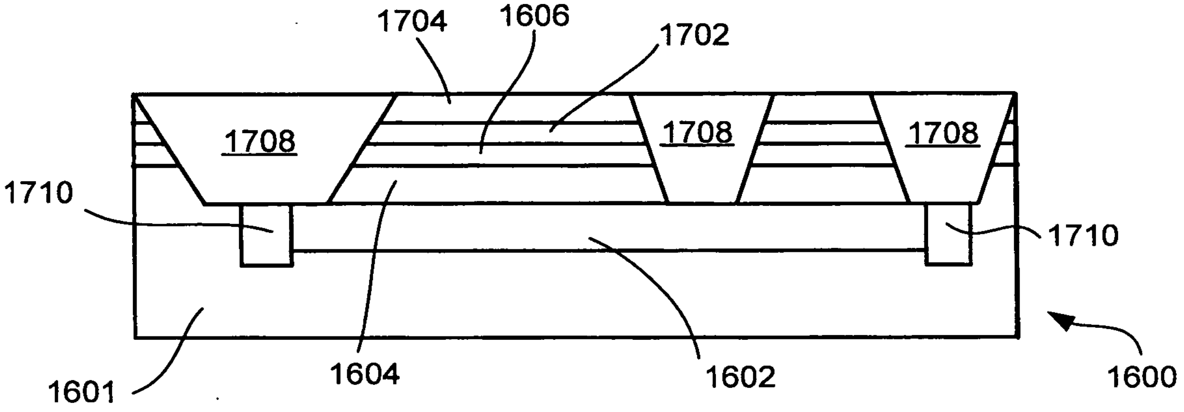

FIG. 17

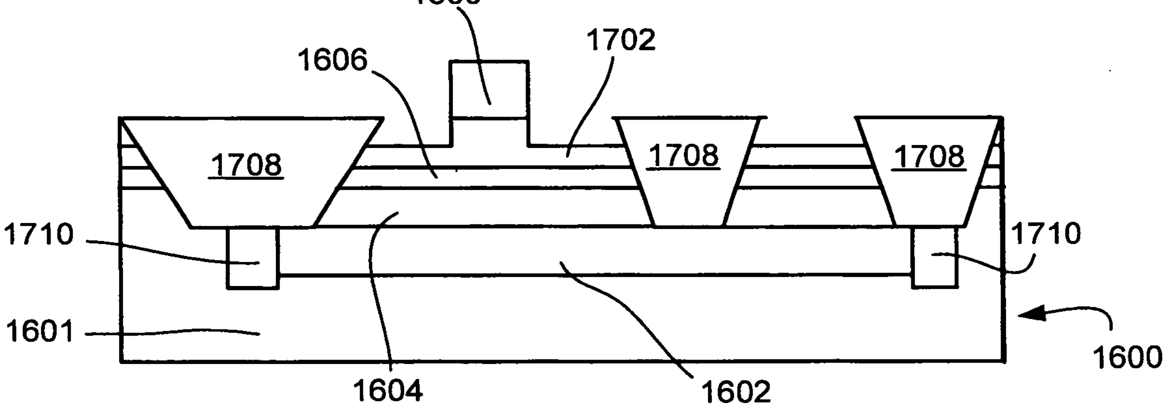

FIG. 18

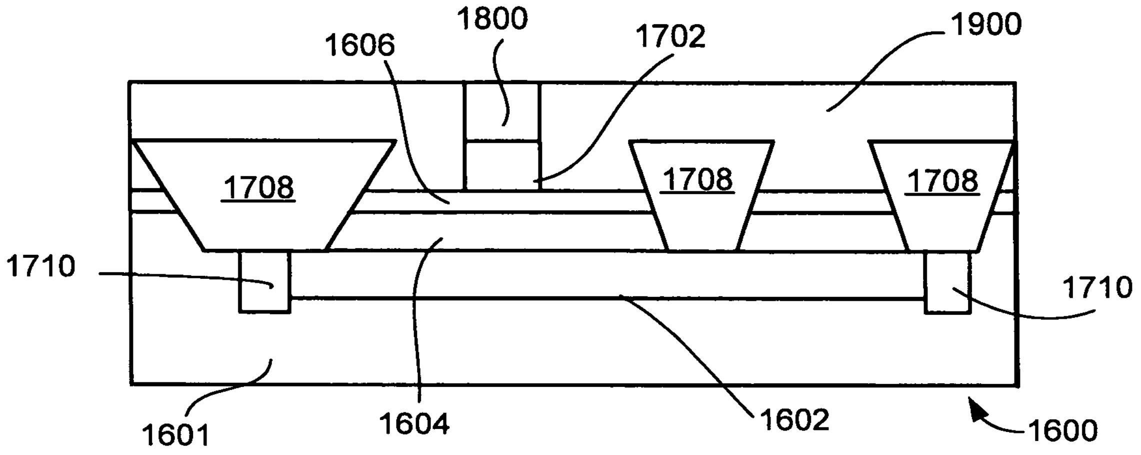

FIG. 19

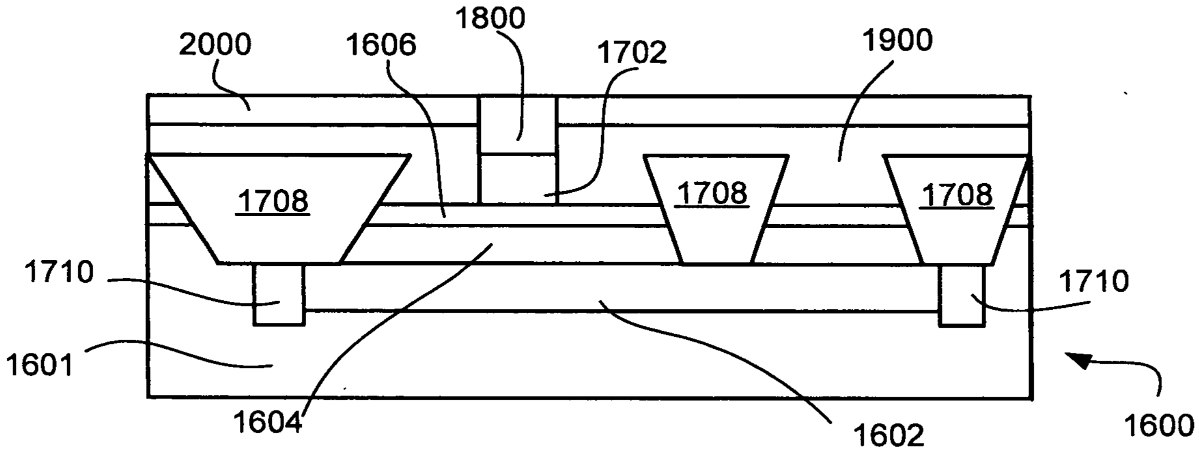

FIG. 20

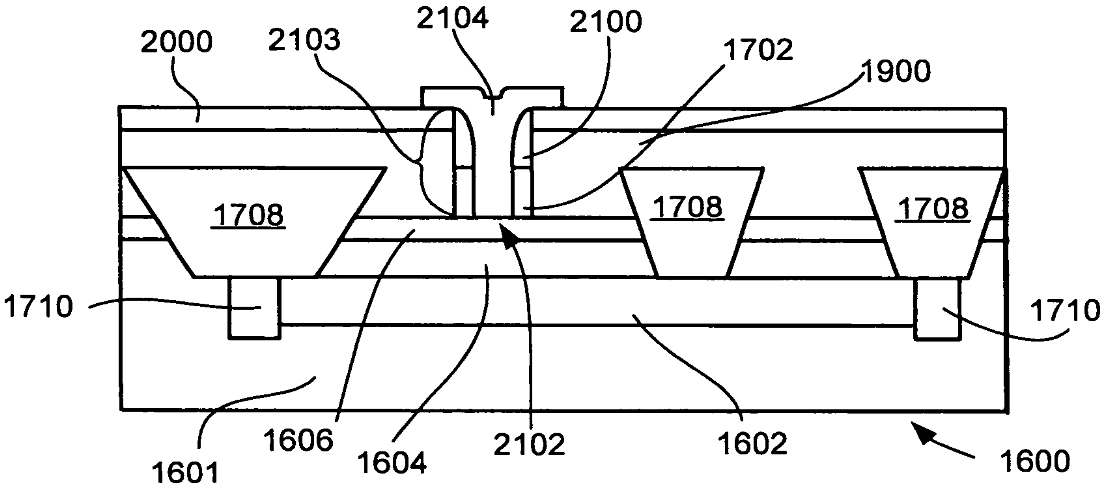

FIG. 21

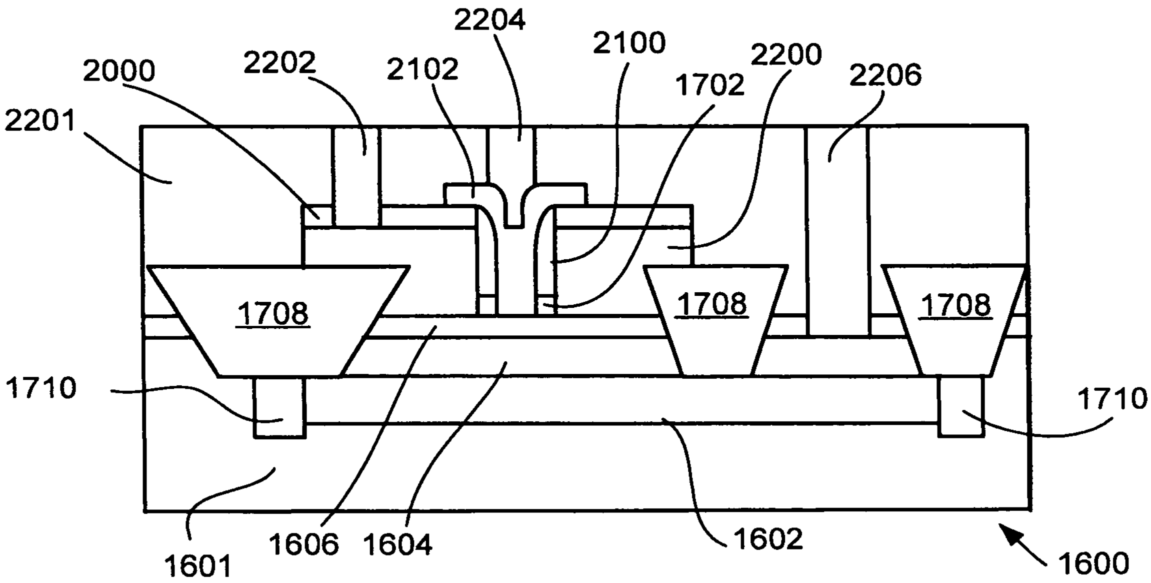

FIG. 22

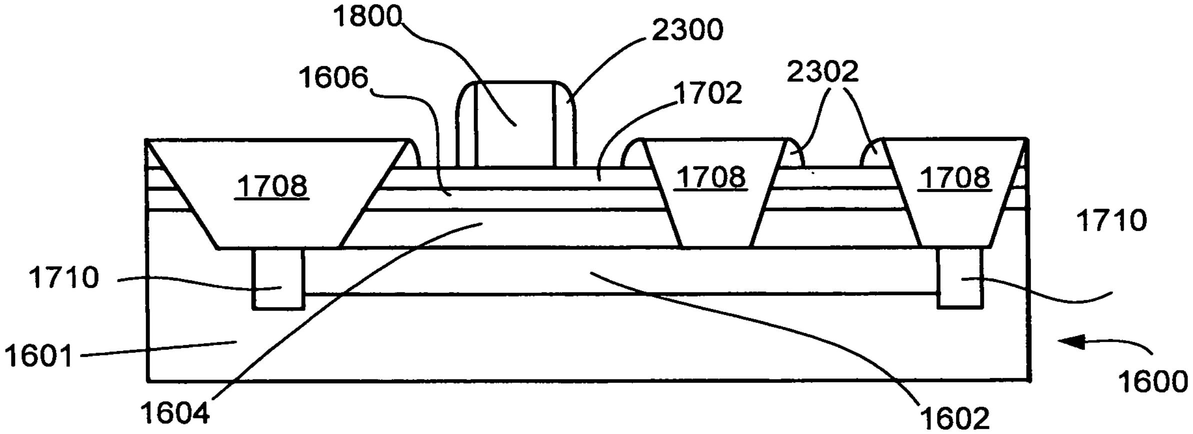

FIG. 23

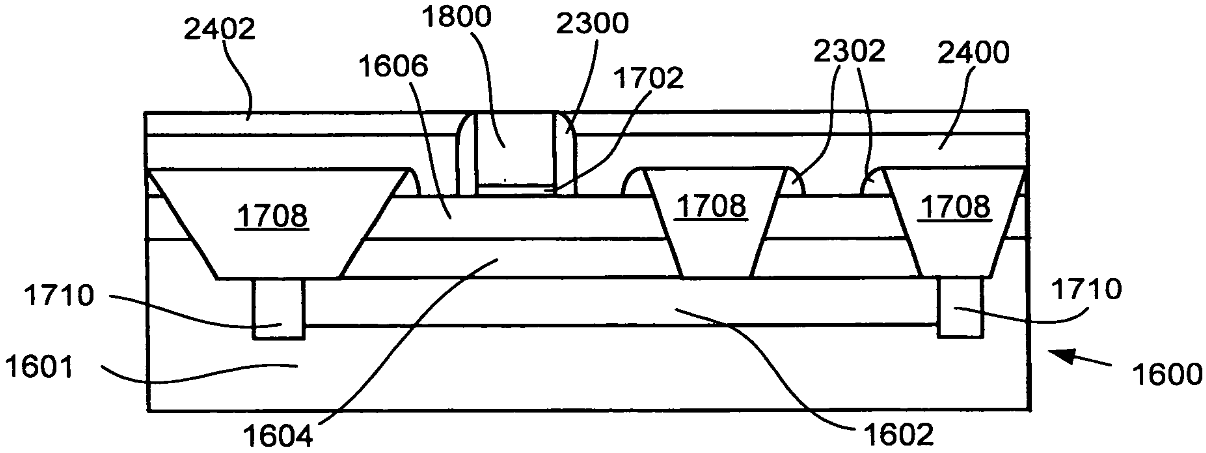

FIG. 24

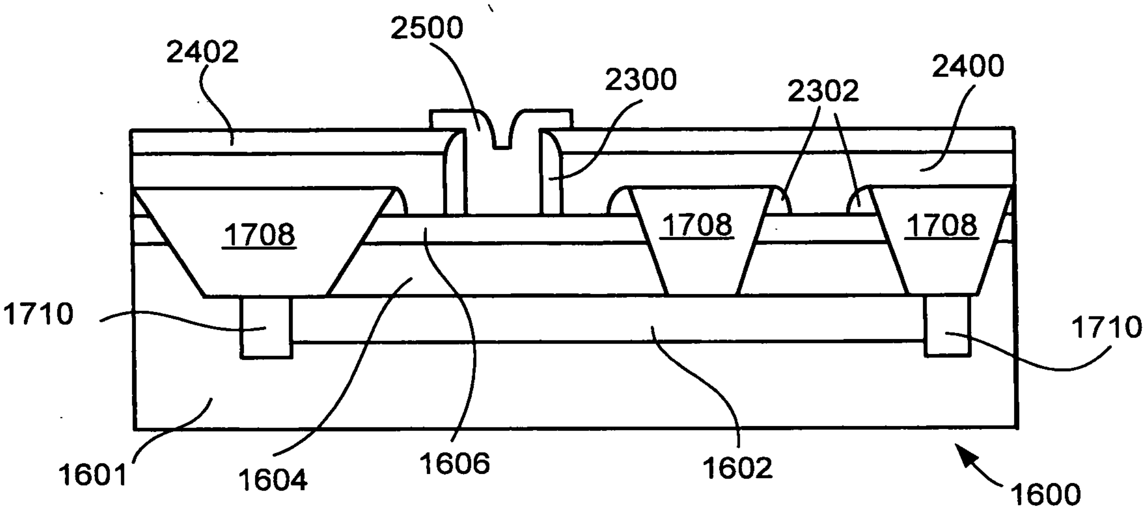
2500
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FIG. 25

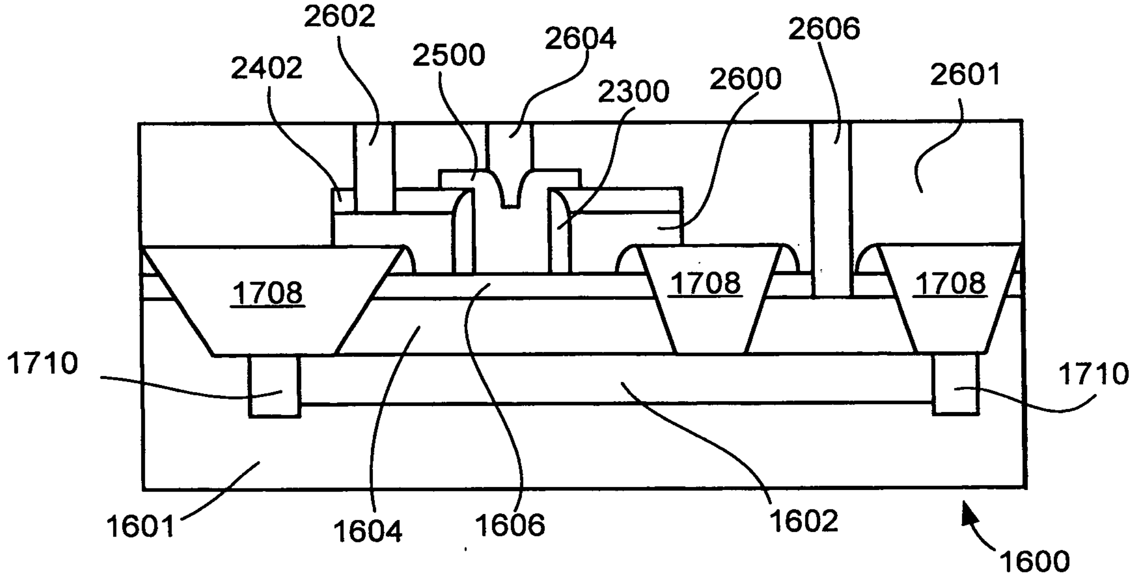
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FIG. 26

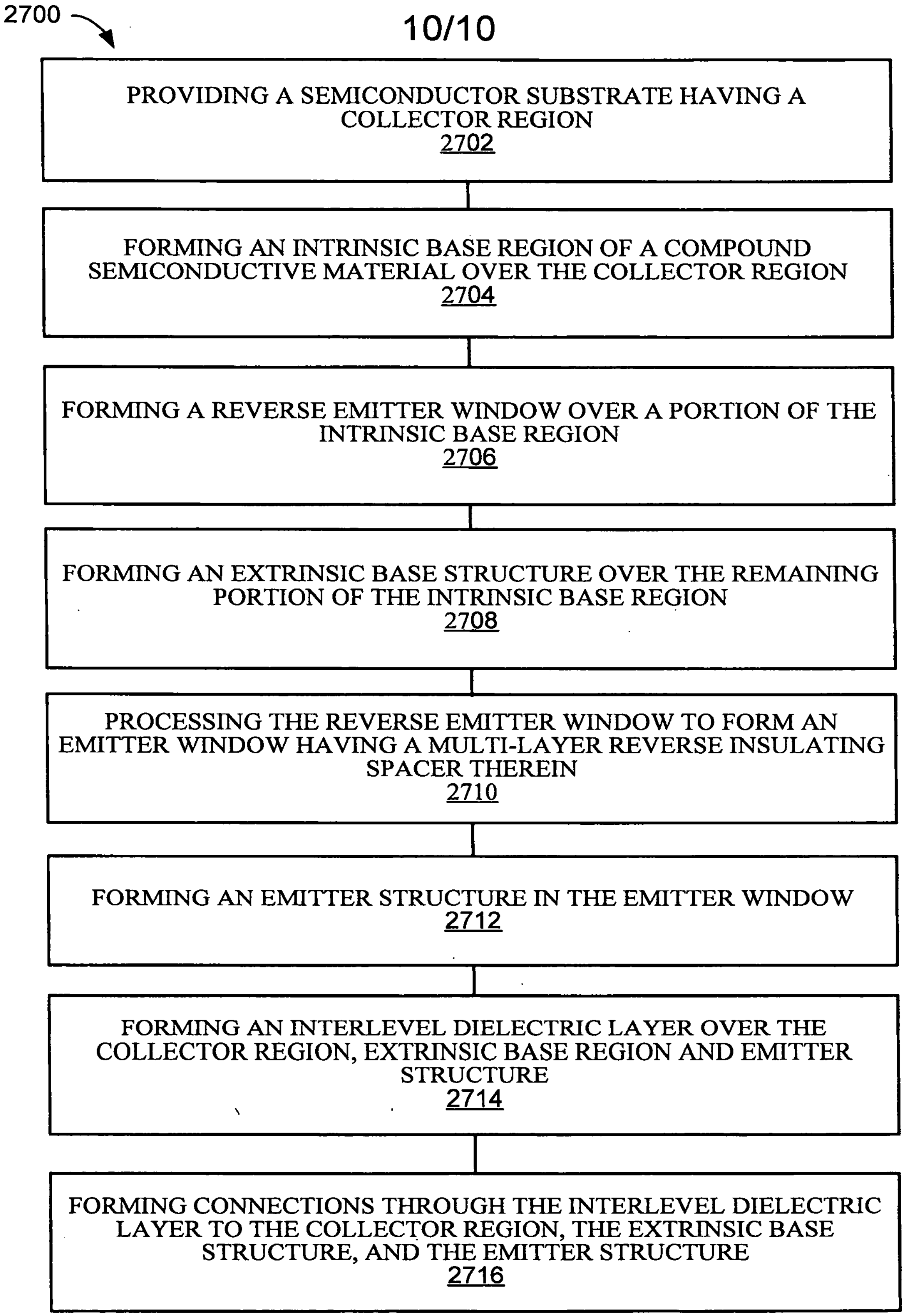
2700
PROVIDING A SEMICONDUCTOR SUBSTRATE HAVING A COLLECTOR REGION
2702
FORMING AN INTRINSIC BASE REGION OF A COMPOUND SEMICONDUCTIVE MATERIAL OVER THE COLLECTOR REGION
2704
FORMING A REVERSE EMITTER WINDOW OVER A PORTION OF THE INTRINSIC BASE REGION
2706
FORMING AN EXTRINSIC BASE STRUCTURE OVER THE REMAINING PORTION OF THE INTRINSIC BASE REGION
2708
PROCESSING THE REVERSE EMITTER WINDOW TO FORM AN EMITTER WINDOW HAVING A MULTI-LAYER REVERSE INSULATING SPACER THEREIN
2710
FORMING AN EMITTER STRUCTURE IN THE EMITTER WINDOW
2712
FORMING AN INTERLEVEL DIELECTRIC LAYER OVER THE COLLECTOR REGION, EXTRINSIC BASE REGION AND EMITTER STRUCTURE
2714
FORMING CONNECTIONS THROUGH THE INTERLEVEL DIELECTRIC LAYER TO THE COLLECTOR REGION, THE EXTRINSIC BASE STRUCTURE, AND THE EMITTER STRUCTURE
2716

FIG. 27